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[METHOD OF ASSESSING POTENTIAL FOR CHARGING DAMAGE IN SOI DESIGNS AND STRUCTURES FOR ELIMINATING POTENTIAL FOR DAMAGE]

Abstract

Disclosed is a method and structure for altering an integrated circuit design having silicon over insulator (SOI) transistors. The method/structure prevents damage from charging during processing to the gate of SOI transistors by tracing electrical nets in the integrated circuit design, identifying SOI transistors that may have a voltage differential between the source/drain and gate as potentially damaged SOI transistors (based on the tracing of the electrical nets), and connecting a shunt device across the source/drain and the gate of each of the potentially damaged SOI transistors. Alternatively, the method/structure provides for connecting compensating conductors through a series device.